

CLAIM AMENDMENTS

1. (Previously Presented) A high-frequency semiconductor device comprising:
a substrate;
an Si MOS transistor on the substrate; and
m lateral polysilicon diodes on the substrate, each of the m lateral polysilicon diodes having a forward direction and a reverse direction, wherein
the m lateral polysilicon diodes are connected in series in the forward direction between a high-frequency I/O signal line and an externally supplied voltage, VDD,
a reverse bias voltage impressed on each of the m lateral polysilicon diodes is smaller than 1.1 volts, and
m is an integer greater than 1.
2. (Previously Presented) A high-frequency semiconductor device comprising:
a substrate;
an Si MOS on the substrate; and
n lateral polysilicon diodes on the substrate, each of the n lateral polysilicon diodes having a forward direction and a reverse direction, wherein
the n lateral polysilicon diodes are connected in series in the forward direction, between ground, GND, and a high-frequency I/O signal line,
a reverse bias voltage impressed on each of the n lateral polysilicon diodes is smaller than 1.1 volts, and
n is an integer greater than 1.
3. (Previously Presented) A high-frequency semiconductor device comprising:
a substrate;
an Si MOS transistor on the substrate; and
m lateral polysilicon diodes on the substrate, each of the m lateral polysilicon diodes having a forward direction and a reverse direction, the m polysilicon diodes being connected in series in the forward direction between a high-frequency I/O signal line and an externally supplied voltage, VDD, and n lateral polysilicon diodes on the substrate, each of the n lateral polysilicon diodes having a forward direction and a reverse direction, the n polysilicon diodes being connected in series between the ground, GND, and the high-frequency I/O signal line, wherein
m and n are positive integers;
 $VDD/(n+m)$ is smaller than 1.1 volts, and
at least one of m and n is greater than 1.

4. (Previously Presented) The high-frequency semiconductor device of Claim 3, wherein no lateral polysilicon diode is connected to any signal line other than the high frequency I/O signal line.

Claims 5 and 6 (Cancelled).

7. (Currently Amended) ~~The~~ A high-frequency semiconductor device ~~of claim 5~~ comprising:

a substrate;

an Si MOS transistor on the substrate;

a first lateral polysilicon diode on the substrate, the first lateral polysilicon diode having a forward direction and a reverse direction, wherein the first lateral polysilicon diode connects, in the forward direction, a high-frequency I/O signal line to an externally supplied voltage VDD; and

a capacitor having lower and upper polysilicon electrodes, wherein the first lateral polysilicon diode and the lower electrode of the capacitor share a single first polysilicon layer, the MOS transistor has a polysilicon gate from a second polysilicon layer, the first and second polysilicon layers having at least one of (i) different dopant impurity concentrations and (ii) different thicknesses, and the polysilicon layer of the upper electrode of the capacitor covers a PN junction of the first lateral polysilicon diode.

8. (Currently Amended) ~~The~~ A high-frequency semiconductor device ~~of claim 5~~ comprising:

a substrate;

an Si MOS transistor on the substrate;

a first lateral polysilicon diode on the substrate, the first lateral polysilicon diode having a forward direction and a reverse direction, wherein the first lateral polysilicon diode connects, in the forward direction, a high-frequency I/O signal line to an externally supplied voltage VDD; and

a capacitor having lower and upper polysilicon electrodes, wherein the first lateral polysilicon diode and the lower electrode of the capacitor share a single first polysilicon layer, the MOS transistor has a polysilicon gate from a second polysilicon layer, the first and second polysilicon layers having at least one of (i) different dopant impurity concentrations and (ii) different thicknesses, and the capacitor includes a dielectric layer and the dielectric layer covers a PN junction of the first lateral polysilicon diode.

Claims 9-13 (Cancelled).

14. (Currently Amended) ~~The~~ A high-frequency semiconductor device ~~of claim 13,~~ comprising:

a substrate;

an Si MOS transistor on the substrate;

a first lateral polysilicon diode on the substrate, the first lateral polysilicon diode having a forward direction and a reverse direction, wherein the first lateral polysilicon diode connects, in the forward direction, ground, GND, to a high-frequency I/O signal line; and

a capacitor having lower and upper polysilicon electrodes, wherein the first lateral polysilicon diode and the lower electrode of the capacitor share a single first polysilicon layer, the MOS transistor has a polysilicon gate from a second polysilicon layer, the first and second polysilicon layers having at least one of (i) different dopant impurity concentrations and (ii) different thicknesses, and the polysilicon layer of the upper electrode of the capacitor covers a PN junction of the first lateral polysilicon diode.

15. (Currently Amended) ~~The~~ A high-frequency semiconductor device ~~of claim 13,~~ comprising:

a substrate;

an Si MOS transistor on the substrate;

a first lateral polysilicon diode on the substrate, the first lateral polysilicon diode having a forward direction and a reverse direction, wherein the first lateral polysilicon diode connects, in the forward direction, ground, GND, to a high-frequency I/O signal line; and

a capacitor having lower and upper polysilicon electrodes, wherein the first lateral polysilicon diode and the lower electrode of the capacitor share a single first polysilicon layer, the MOS transistor has a polysilicon gate from a second polysilicon layer, the first and second polysilicon layers having at least one of (i) different dopant impurity concentrations and (ii) different thicknesses, and the capacitor includes a dielectric layer and the dielectric layer covers a PN junction of the first lateral polysilicon diode.

Claim 16 (Cancelled).